

CLAIMS

What is claimed is:

- 1) A circuit for applying power to an on-chip cache memory array comprising:
 - a switch in series with a power supply and said on-chip cache memory array;
 - a PMU electrically connected to said on-chip cache memory array ;
 - a software application electrically connected to said PMU;wherein said switch may be opened or closed by said PMU.
- 2) The circuit as in Claim 1 wherein said switching device is connected between a negative terminal of said on-chip cache memory array and GND of said power supply.
- 3) The circuit as in Claim 2 wherein said switching device is a MOSFET.
- 4) The circuit as in Claim 2 wherein said switching device is a bipolar transistor.
- 5) The circuit as in Claim 1 wherein said switching device is connected between a positive terminal of said on-chip cache memory array and VDD of said power supply.
- 6) The circuit as in Claim 5 wherein said switching device is a MOSFET.
- 7) The circuit as in Claim 5 wherein said switching device is a bipolar transistor.

8) A circuit for applying power to an on-chip cache memory array comprising:

a switch in series with a power supply and said on-chip cache memory array;

a PMU electrically connected to said on-chip cache memory array ;

wherein said switch may be opened or closed by said PMU.

9) The circuit as in Claim 8 wherein said switching device is connected between a

negative terminal of said on-chip cache memory array and GND of said power supply.

10) The circuit as in Claim 9 wherein said switching device is a MOSFET.

11) The circuit as in Claim 9 wherein said switching device is a bipolar transistor.

12) The circuit as in Claim 8 wherein said switching device is connected between a

positive terminal of said on-chip cache memory array and VDD of said power supply.

13) The circuit as in Claim 12 wherein said switching device is a MOSFET.

14) The circuit as in Claim 12 wherein said switching device is a bipolar transistor.

15) A circuit for applying power to an on-chip cache memory array comprising:

a switch in series with a power supply and said on-chip cache memory array;

a software application electrically connected to a PMU ;

wherein said switch may be opened or closed by said PMU.

16) The circuit as in Claim 15 wherein said switching device is connected between a
negative terminal of said on-chip cache memory array and GND of said power
supply.

17) The circuit as in Claim 16 wherein said switching device is a MOSFET.

18) The circuit as in Claim 16 wherein said switching device is a bipolar transistor.

19) The circuit as in Claim 15 wherein said switching device is connected between a
positive terminal of said on-chip cache memory array and VDD of said power supply.

20) The circuit as in Claim 19 wherein said switching device is a MOSFET.

21) The circuit as in Claim 19 wherein said switching device is a bipolar transistor.

22) A method for applying power to a on-chip cache memory array comprising:

electrically connecting a switch between a power supply and said on-chip cache
memory array;

electrically connecting a PMU to said on-chip cache memory array;

electrically connecting a software application to said PMU;

wherein said switch may be opened or closed by said PMU.

23) The method as in Claim 22 wherein said switching device is connected between a
negative terminal of said on-chip cache memory array and GND of said power
supply array.

4
24) The method as in Claim 23 wherein said switching device is a MOSFET.

2
25) The method as in Claim 23 wherein said switching device is a bipolar transistor.

2
26) The method as in Claim 22 wherein said switching device is connected between a
2 positive terminal of said on-chip cache memory array and VDD of said power supply.

2
27) The method as in Claim 26 wherein said switching device is a MOSFET.

2
28) The method as in Claim 26 wherein said switching device is a bipolar transistor.

2
29) A method for applying power to an on-chip cache memory array comprising:
2 electrically connecting a switch between a power supply and said on-chip cache
memory array;
4 electrically connecting a PMU to said on-chip cache memory array;
wherein said switch may be opened or closed by said PMU.

6
30) The method as in Claim 29 wherein said switching device is connected between a
2 negative terminal of said on-chip cache memory array and GND of said power
supply array.

4
31) The method as in Claim 30 wherein said switching device is a MOSFET.

2
32) The method as in Claim 30 wherein said switching device is a bipolar transistor.

2

33) The method as in Claim 29 wherein said switching device is connected between a
4 positive terminal of said on-chip cache memory array and VDD of said power supply.

2

34) The method as in Claim 33 wherein said switching device is a MOSFET.

2

35) The method as in Claim 33 wherein said switching device is a bipolar transistor.

2

36) A method for applying power to a cache memory array comprising:

2

electrically connecting a switch between a power supply and said on-chip cache
memory array;

4

electrically connecting a software application to a PMU;

6

wherein said switch may be opened or closed by said PMU.

2

37) The method as in Claim 36 wherein said switching device is connected between a
negative terminal of said on-chip cache memory array and GND of said power
supply array.

4

2

38) The method as in Claim 37 wherein said switching device is a MOSFET.

2

39) The method as in Claim 37 wherein said switching device is a bipolar transistor.

4

40) The method as in Claim 36 wherein said switching device is connected between a
positive terminal of said on-chip cache memory array and VDD of said power
supply.

41) The method as in Claim 40 wherein said switching device is a MOSFET.

42) The method as in Claim 40 wherein said switching device is a bipolar transistor.

2025 RELEASE UNDER E.O. 14176